a semiconductor substrate and (2) a capacitor element connected in series, comprising the steps of:

(a) forming a plurality of first electrodes respectively for the capacitor elements over the gate electrodes of respective MISFETs, said first electrodes being electrically connected to one of said source region and drain region and extending over the gate electrodes;

(b) depositing a dielectric film on said plurality of first electrodes;

(c) depositing a conductive film on said dielectric film;

(d) forming a mask layer having a predetermined pattern larger than each of said plurality of first electrodes in directions which said data lines and said word lines extend, over said conductive film, and

(e) etching both said conductive film and said dielectric film at a portion exposed from said mask layer in order to form second electrodes for the plurality of capacitor elements, wherein said second electrodes are formed in order to be connected as second electrodes of the capacitor elements of the plurality of memory cells.

2. (Amended) A method of producing a semiconductor integrated circuit device according to claim 1, wherein after said etching, said dielectric film exists only under said second electrodes.

4. (Amended) A method of producing a semiconductor integrated circuit device having a plurality of MISFETs arranged in a first direction and in a second

direction which is perpendicular to said first direction, each of said plurality of MISFETs having a gate electrode and a source region and a drain region, and a plurality of capacitor elements each having a first electrode respectively connected to one of the source region and the drain region of a respective one of said plurality of MISFETs, a dielectric film and a second electrode, comprising the steps of:

(a) depositing a first conductive film over a semiconductor substrate;

(b) patterning said first conductive film in order to form a plurality of first electrodes for said plurality of capacitor elements, said plurality of first electrodes being arranged in said first and second directions, each of said plurality of first electrodes extending respectively over gate electrodes of said plurality of MISFETs;

(c) depositing a dielectric film on said plurality of first electrodes;

(d) depositing a second conductive film on said dielectric film; and

(e) etching said second conductive film and said dielectric film in order to form second electrodes for said plurality of capacitor elements and a patterned dielectric film,

wherein said patterned dielectric film has substantially a same pattern as that of the second electrodes and exists only under said second electrodes, said patterned dielectric film not extending over the other of the source region and the drain region of the respective one of the plurality of MISFETs, and

wherein said second electrodes are larger than said plurality of first electrodes in said first and second directions and are formed in order to cover at least each of the one of the source region and the drain region of the plurality of MISFETs.

5. (Amended) A method of producing a semiconductor integrated circuit device having a plurality of MISFETs arranged in a first direction and in a second direction which is perpendicular to said first direction, each of said plurality of MISFETs having a gate electrode and a source region and a drain region, and a plurality of capacitor elements each having a first electrode respectively connected to one of the source region and the drain region of a respective one of said plurality of MISFETs, a dielectric film and a second electrode, comprising the steps of:

(a) forming the plurality of first electrodes for the capacitor elements over a semiconductor substrate, each of the plurality of first electrodes extending respectively over gate electrodes of said plurality of MISFETs;

(b) depositing a dielectric film on said plurality of first electrodes;

(c) depositing a conductive film on said dielectric film; and

(d) patterning said conductive film and said dielectric film respectively to form second electrodes and a patterned dielectric film,

wherein said patterned dielectric film has substantially a same pattern as that of said second electrodes, said patterned dielectric film not extending over the other of the source region and the drain region of each of the plurality of MISFETs, and

wherein said second electrodes are larger than said plurality of first electrodes in said first and second directions and are formed in order to cover at least each gate electrode of said plurality of MISFETs.

6. (Amended) A method of producing a semiconductor integrated circuit device according to claim 5, wherein said second electrodes cover both said patterned dielectric film and the plurality of first electrodes.

7. (Amended) A method of producing a semiconductor integrated circuit device according to claim 5, wherein said second electrodes cover the plurality of first electrodes.

Please add the following new claims to the application:

--8. A method of producing a semiconductor integrated circuit device having word lines, data lines and a plurality of memory cells each connected to one of the word lines and one of the data lines, each of said plurality of memory cells having (1) a MISFET having a gate electrode and a source region and a drain region on a semiconductor substrate and (2) a capacitor element connected to series, comprising the steps of:

(a) forming a plurality of first electrodes for said capacitor elements over the gate electrodes of the MISFETs, each of said plurality of first electrodes being electrically connected to one of said source region and drain region and extending over the gate electrode;

(b) depositing a dielectric film on said plurality of first electrodes;

(c) depositing a conductive film on said dielectric film;

(d) forming a mask layer having a predetermined pattern larger than each of said plurality of first electrodes in directions which said data lines and said word lines extend, over said conductive film; and

(e) etching both said conductive film and said dielectric film at a portion exposed from said mask layer in order to form second electrodes for the plurality of capacitor elements,

wherein said etching also etches said dielectric film over the other of said source and drain regions of said MISFETs, and

wherein said second electrodes are formed in order to be connected as second electrodes of the capacitor elements of the plurality of memory cells.

9. A method of producing a semiconductor integrated circuit device according to claim 8, wherein after said etching, said dielectric film exists only under said second electrodes.

10. A method of producing a semiconductor integrated circuit device according to claim 8, wherein said dielectric film has at least a double-layer structure of a silicon nitride film and a silicon oxide film stacked on the silicon nitride film.

11. A method of producing a semiconductor integrated circuit device according to claim 8, wherein each of the second electrodes is formed so as to be connected as a second electrode of more than one capacitor element of the memory cells.

12. A method of producing a semiconductor integrated circuit device according to claim 11, wherein each of the second electrodes is formed so as to be connected as a second electrode of capacitor elements of a memory cell and an adjacent memory cell.

13. A method of producing a semiconductor integrated circuit device according to claim 1, wherein each of the second electrodes is formed so as to be connected as a second electrode of more than one capacitor element of the memory cells.

14. A method of producing a semiconductor integrated circuit device according to claim 13, wherein each of the second electrodes is formed so as to be connected as a second electrode of capacitor elements of a memory cell and an adjacent memory cell.--